At page 1, line 2, please add the following **new section** to the specification:

RELATED APPLICATIONS

This application claims priority to United States Provisional Patent Application Number 60/455,282, entitled "Recognition Device and System", filed on March 17, 2003, and which is hereby incorporated herein in its entirety.

At page 6, line 1, please **replace** the "BRIEF DESCRIPTION" **section** with the following (marked up to show changes):

BRIEF DESCRIPTION OF THE DRAWINGS ~~(FIGURES 1-5 ARE FOUND IN APPENDIX A; FIGURE A IS ATTACHED)~~

These and other features of the invention will be understood from the description and claims below, taken together with the figures showing illustrative embodiments, wherein:

Figure 1 illustrates the database structure and flow of information in one embodiment of an object identification system of the present invention;

Figure 1A illustrates diagrammatically a system of one embodiment of the invention and shows the relationship between a Hierarchical Memory (HM) module, a Selective Attention Module (SAM) and a Front End Module (FEM).

Figure 2 illustrate rules of connectivity between levels for the system of Figure 1;

Figure 3 illustrates detailed steps in the recognition process and iterative accumulation of information at all levels of the system shown in Figures 1 and 2;

Figures 4A and 4B illustrate time-dependent changes during recognition, with and without contextual information for a bidirectional mismatch feature window;

Figure 5 charts a comparison of efficiency in producing recognition, of different feature selection regimens;

~~Figure A illustrates the relationship between the Hierarchical Memory (HM) module, the Selective Attention Module (SAM) and the Front End Module (FEM).~~

At page 1, line 9, before the title "Example of the recognition process" please add the following **new paragraphs** to the specification:

Architecture for a recognition processor system or device: A system or device of the invention for carrying out the processing described above may have a Hierarchical Memory (HM) module, a Selective Attention Module (SAM) and a Front End Module (FEM). Bidirectional arrows between modules indicate the ability to process parallel signals through the nodal network interface connections in both Bottom-Up (B-U) and Top-Down (T-D) directions. The "Raw Input" sensor array (or feature array) signal enters B-U into the FEM. The FEM may perform scaling and other transformations to this B-U input array. A normalized array is fed B-U from the FEM into the B-U input of the SAM.

The SAM is responsible for selecting which signal from the FEM is to be transmitted next to the B-U input of the HM module, where multi-level, bidirectional parallel processing occurs. The SAM uses its B-U and T-D input in an algorithm that selects which B-U inputs from the FEM to gate upwards to the HM.

The information in the HM is represented in multiple hierarchical levels though selective connections between nodes at different levels. Nodes at the highest level start out active and are progressively silenced. This represents an integration of information over multiple samples made by the SAM. The active T-D stream represents high-level (contextual) constraints and allows computation of a measure of feature probability, based on the still active nodes at the highest level. The B-U stream represents what is "there" as reported by the input array.